20-GHz INP-HBT Voltage-Controlled Oscillator with Wide Tuning Range

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***Abstract* — This paper presents the design and implementation of a 20-GHz-band differential VCO using InP HBT process technology. Aimed at 20- or 40-Gb/s fiber optic applications, the design is based on a single-stage feedback amplifier with no intentional L or C. The salient features of the proposed VCO are wide frequency tuning range compared to LC oscillators, and low power consumption and transistor count compared to ring-oscillator counterparts. The implemented VCO has an adjustable frequency range from 13.75 GHz to 21.5 GHz and provides two complementary outputs. Total power consumption at 18.6 GHz is 130 mW, while the phase noise is -87.6 dBc/Hz measured at 1 MHz offset.**

I. INTRODUCTION

The ever increasing demand for bandwidth in data communication systems, e.g. synchronous optical networks (SONET), has motivated research on very high-speed devices and circuits. New generation of optical carrier systems are designed for data rates of 20 Gb/s, 40 Gb/s and higher, and are beyond the reach of today's silicon CMOS or conventional bipolar processes. Indium-Phosphide (InP) technology offers an attractive choice for high-speed optoelectronic integrated circuits (OEICs) due to its higher speed and the availability of optoelectronic transducers (E/O, O/E) compatible with fiber optic systems. InP Heterojunction Bipolar Transistors (HBTs) have shown device f_T exceeding 150 GHz and benefit from low loss and low-parasitic interconnects due to the semi-insulating substrate. Other features of InP HBTs are low $1/f$ noise, low V_{BE} turn-on voltage compared to GaAs counterparts, and high-efficiency devices for oscillators [1] - [3].

This paper presents the design and implementation of a differential InP-HBT VCO for a 20-Gb/s or 40-Gb/s (OC-768) SONET/ SDH system. The VCO must operate over process and temperature variations and exhibit a wide adjustable frequency range. VCOs with center frequencies of 20 GHz and 40 GHz are two options for a 40-Gb/s system, depending on the architecture used for clock and data recovery. A 20-GHz design is employed here. The design is fully-differential and provides two outputs with 180° phase difference and low skew and jitter. The two complementary outputs can be used with two parallel latches to retime data stream on both positive and negative clock edges, effectively creating a 40-Gb/s data interface. The proposed VCO can be used in clock-and-data recovery PLL (RX side) as well as clock synthesizer (TX side) of a fiber optic system. The specified supply voltage and maximum power consumption are -3.3V and 200mW, respectively.

II. INP-HBT PROCESS TECHNOLOGY

The InP process considered provides high-speed NPN heterojunction bipolar transistors with single 1.5-μm emitter strip width. HBTs with emitter lengths of 6 μm to 15 μm are used in the proposed design. Unity current gain frequency (f_T) of the HBTs peaks at a collector current density of 1 $mA/\mu m^2$ which is also the maximum allowable current density for these devices. Thus, in practice HBTs must operate at current levels safely below their peak-f_T point. To avoid breakdown, maximum V_{CE} is maintained at 2V for dc quiescent point design and 3.3V when signal swing is considered. At a typical collector current density of 0.7 $mA/\mu m^2$ and collector-emitter voltage of 1.2V, estimated f_T is about 100 GHz. Two metallization layers are used for interconnections with minimum metal pitch of 7 μm. Lossy transmission lines consisting of top metal, 75-μm semi-insulating InP substrate and backside ground plane are also available. Other available components in this technology are NiCr resistors, metal-insulator-metal (MIM) capacitors and Schottky diodes. All active and passive components have process- and geometry-scalable models [4] with built-in parasitic elements (RLC), and self-heating and breakdown models for the HBTs.

III. WIDE-RANGE VCO DESIGN

The proposed VCO design is based on regenerative feedback applied to a differential amplifier. The idea is to obtain 180° frequency-dependent phase shift within a single-stage differential cell relying on poles and zeros obtained in a cascode configuration followed by emitter-follower buffers. To create the positive feedback, another 180° phase shift is obtained by swapping the differential feedback lines from the output to the input of the amplifier. The proposed circuit can be treated as a feedback amplifier, or as a 'single-stage' ring oscillator. Ultra fast InP HBTs push the main pole of the amplifier to a very high frequency, effectively close to secondary poles and right-half-plane zeros, thus making it possible to achieve 180° phase from the differential cell at a frequency where small signal gain is above 0 dB. In this manner, a 'short' ring oscillator is realized with a single buffered stage, hence saving on power consumption and device count.

Figure 1 shows the schematic of the NPN-only differential-core oscillator. It consists of a differential input pair, a cascode (common-base) pair and an emitter-follower buffer pair. The simulated open-loop frequency response of such a differential cell for a midband control voltage is shown in Fig. 2. In the simulation, the differential cell is opened at points 'A' and 'B' (*cf.* Fig. 1) and the output is loaded by a similar stage (in feedback configuration the cell will be loaded by its own inputs). The loading effect of an output buffer stage is also included in the simulation. Figure 2 reveals that a frequency-dependent phase shift of -180° occurs at about 19 GHz while the small-signal gain at this frequency is around + 2 dB. Therefore, the gain-phase conditions are achieved for oscillation around this frequency. Additional simulations indicate that when control voltage $(V_b - V_{ee})$ is swept from 0.9V to 1.1V, the gain magnitude is increased and the 180° crossing point in the phase plot is shifted towards higher frequencies. The gain-bandwidth product is also increased.

The operation of the differential cell in Fig. 1 as an oscillator is guaranteed by the gain-phase conditions. An increase in tail current increases f_T and also the charging current of parasitic capacitances, thus increasing the frequency of the oscillation. This is achieved by changing the control voltage that simultaneously adjusts the tail current of the differential cascode as well as the bias currents of the emitter-follower pair. Steady-state frequency of the closed-loop oscillation can be different from the small-signal prediction due to nonlinear effects. The oscillator stabilizes at a frequency where 'large-signal' gain is 0 dB. The oscillation frequency is determined through transient simulations that take into account large-signal nonlinear effects. For this circuit, the oscillation frequency in transient simulation is about 20 GHz.

The complete VCO circuit consists of an input voltage-to-current (V/I) converter, the core oscillator, and a differential output driver stage. The complete circuit schematic is shown in Fig. 3(a). The input V/I converter, consisting of resistors and a diode-connected HBT, creates a reference current proportional to VCO's input control voltage. The reference current is mirrored to the tail current of the differential pair and to the bias current of the emitter-follower feedback HBTs. The output driver is a differential common-emitter amplifier driving 50-Ω resistors both on chip and off chip (equivalent load is 25 Ω on each collector). All capacitors shown in Fig. 3(a) are parasitics backannotated from the layout, except for two metal-insulator-metal (MIM) capacitors bypassing supply and the base of cascode HBTs.

The layout of the InP VCO consists of a symmetrical configuration of 13 HBTs, 13 NiCr resistors and 2 MIM capacitors. The transistor count is one third of that in a three-stage InP ring oscillator [5]. The cell size is 620 μm × 318 μm, or about 0.2 mm^2. The effect of parasitic interconnect capacitors (i.e. M1-Substrate, M2-Substrate, M1-M2 air-bridge) is taken into account by extracting the area and perimeter of overlap geometries; the dominant component in most cases is the fringe (perimeter) capacitance. Through preliminary transient simulations of the VCO, those nodes with maximum *sensitivity to parasitic capacitance* (max. $\Delta f / \Delta C$) were identified and ranked accordingly. The physical layout was then optimized to insert minimum metal capacitance on the most sensitive nodes.

Figure 3(b) shows the simulation testbench of the VCO. The output drivers are connected via wide (low-impedance) transmission lines on chip to output signal pads. The 50-Ω resistors in the testbench represent external terminations, while on-chip 50-Ω resistors have been included inside the VCO on the collector of output HBTs. The final circuit was characterized via backannotated (postlayout) transient simulations. A robust oscillation was sustained under all simulated process models (Nominal, Fast, Slow) and control voltages varying from -2V to 0V. Temperature simulations were performed in a range from 0°C to 100°C. While a temperature rise decreases the output frequency, the oscillation is maintained with a fairly constant output amplitude. Peak-to-peak amplitude of an output node at midband varied from 460mV to 425mV when temperature parameter (TEMPDC) was increased from 0°C to 100°C.

IV. IMPLEMENTATION

The proposed wide-range VCO circuit was implemented using the InP-HBT process described in Section 2. Figure 4 shows the photomicrogaph of the InP VCO. The implemented test chip contains two such VCO circuits

(with slight design variations in supply and bias), high-frequency signal pads, as well as standard pads for supply, ground and control input. The signal pads have smaller size ($60 \times 60\ \mu m^2$) and exhibit a capacitive loading under 20 fF. The chip die size is $1.2 \times 1.2\ mm^2$. The testing was performed on wafers using a 50-Ω RF prober. Maximum frequency of oscillation of the VCO, measured on different InP wafers, varied from $18\ GHz$ to $23\ GHz$. Detailed measurements are presented here for an average die with maximum VCO frequency of $21.5\ GHz$.

Figure 5 shows the measured output frequency and output power (dashed line) of the InP VCO vs. input control voltage. The measured output frequency was adjustable from 13.75 GHz to 21.5 GHz using a control voltage of $-1.8V$ to 0V. The average gain of the VCO was about $4.3\ GHz/V$. The VCO exhibits a wide tuning range of 45%, as compared to tuning ranges of 1% - 15% reported for VCOs with LC-tuned or multivibrator oscillators [6], [3]. The two outputs have 180° phase difference. The measured power obtained at each output varied from $-2.8\ dBm$ to $-8\ dBm$ over the input control range, as compared to a typical mid-range simulation of -3 dBm.

Figure 6 shows the output spectrum of the VCO for a mid-range oscillation frequency of 18.56 GHz. The measured phase noise, as indicated on the spectrum, was -87.6 dBc/Hz at 1 MHz offset to the carrier. The phase noise is comparable to those reported for ring oscillators. However, compared to conventional (multi-stage) ring oscillators, the proposed VCO is advantageous in terms of power consumption and transistor count as it is formed by a single-stage delay cell. For instance, a three-stage ring oscillator with 10 or 26 GHz frequency options is built with 40 InP-HBTs and consumes 250 mW power [5]. The design proposed in this paper consists of 13 HBTs and has a measured power of 130 mW from -3.3V supply. The measurement includes power dissipation in the input control circuit, the VCO core, and the drivers. The differential core has an approximate power consumption of 80 mW. With a larger supply voltage of V_{ee} = - 4V, a maximum measured frequency of 30.0 GHz was obtained. Future designs are aimed at 40-GHz operation.

V. CONCLUSION

The design and implementation for fiber optic applications of a 20-GHz-band differential VCO was presented. The design is based on positive feedback on a single-stage differential amplifier. The main advantage of the proposed VCO is the wide tunable frequency range which can be used to compensate for process or temperature variations when used within a PLL. Other features include low power and low transistor count compared to conventional ring oscillators. The implemented InP VCO has an adjustable frequency range of 45% from 13.75 GHz to 21.5 GHz. It provides two complementary outputs each delivering a power level of -2.8 dBm to -8 dBm. The total power consumption is 130 mW and the measured phase noise is -87.6 dBc/Hz at 1 MHz offset.

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REFERENCES

[1] B. Jalali and S. J. Pearton (Editors), *InP HBTs: Growth, Processing and Applications*, Artech House Inc., MA, 1995.

[2] M. Wuzer, J. Bock, H. Knapp, W. Zirwas, F. Schumann, A. Felder, "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silicon Bipolar Technology," *IEEE J. Solid-State Circuits*, Vol. 34, No. 9, pp. 1320-1324, 1999.

[3] M. Yung, J. Jensen, R. Walden, M. Rodwell, G. Raghavan, K. Elliott, W. Stanchina, "Highly Integrated InP HBT Optical Receivers," *IEEE J. Solid-State Circuits*, Vol. 34, No. 2, pp. 219-227, 1999.

[4] S. Voinigescu, D. Marchesan, J. Showell, M. Maliepaard, M. Cudnoch, M. Schumacher, M. Herod, D. Walkey, G. Babcock, P. Schvan, R. Hadaway, "Process- and Geometry-Scalable Bipolar Transistor and Transmission Line Models for Si and SiGe MMIC in the 5-22GHz Range," *Int. Electron Devices Meeting (IEDM) Tech. Digest*, pp. 307-310, 1998.

[5] R. Montgomery, D. Humphrey, R. Hamm, F. Ren, R. Malik, R. Kopf, A. Tate, P. Smith, R. Ryan, J. Lin, Y. Chen, "10 and 26 GHz Differential VCOs Using InP HBTs," *IEEE IMTT-S Int. Microwave Symp. Digest*, Vol. 3, pp. 1507-1510, 1996.

[6] M. Soyuer, J. Burghartz, H. Ainspan, K. Jenkins, P. Xiao, A. Shahani, M. Dolan and D. Harame, "An 11-GHz 3-V SiGe Voltage-Controlled Oscillator with Integrated Resonator," *Proc. IEEE Bipolar Circuits & Technology Meeting*, pp. 169-173, 1996.

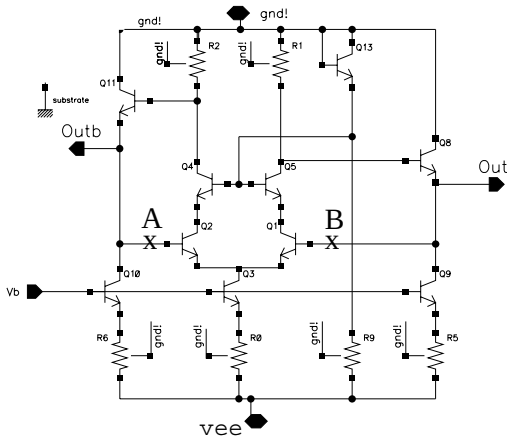


Fig. 1. InP differential cell oscillator

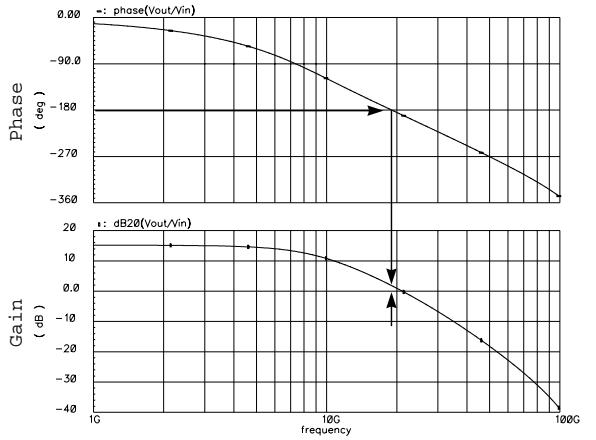
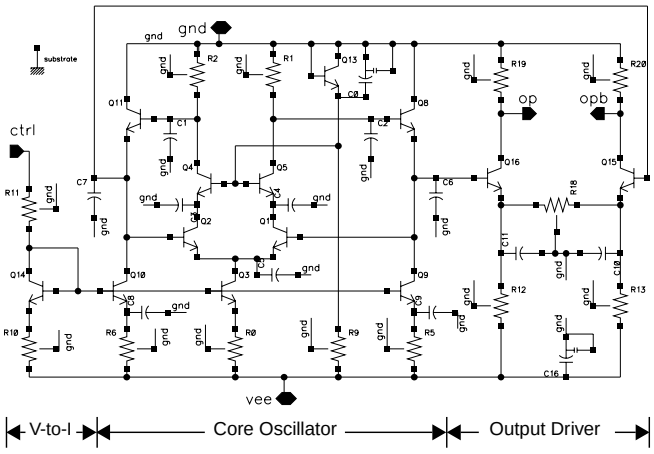
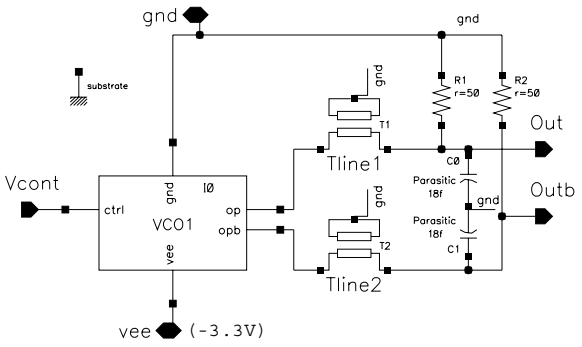


Fig. 2. Open-loop phase plot (top) and gain plot (bottom) of the differential cell.



(a)



(b)

Fig. 3. (a) Complete circuit of the wide-range InP VCO, **(b)** simulation testbench.

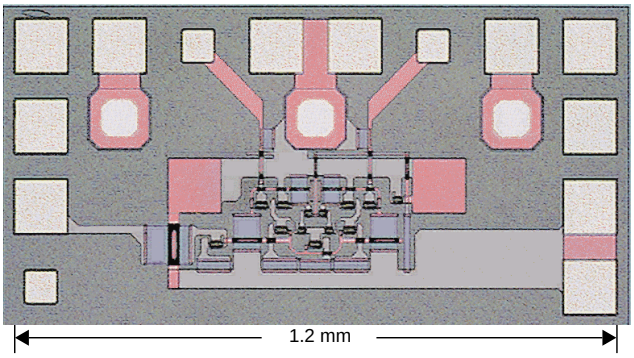


Fig. 4. Photomicrograph of the InP VCO.

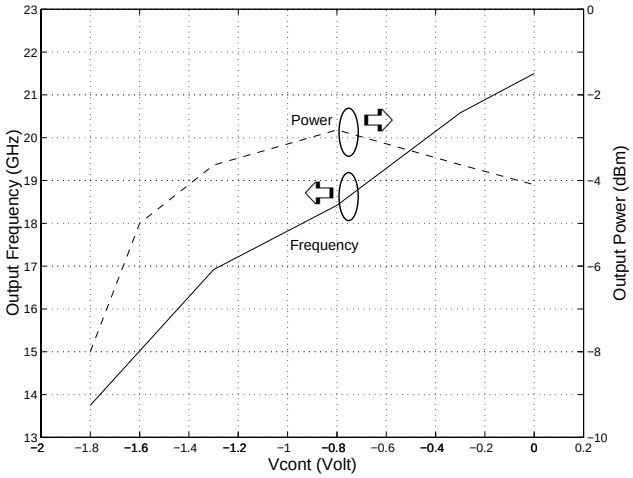


Fig. 5. Measured frequency of the VCO; measured power level (dBm) from each output.

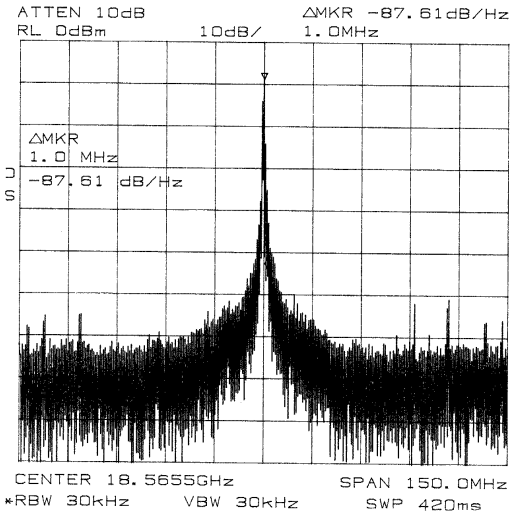


Fig. 6. Output spectrum of the VCO at 18.6 GHz.